ABSTRACT OF THE DISCLOSURE

A process for fabricating high-voltage drain-extension transistors, whereby the transistors are integrated in a semiconductor substrate along with non-volatile memory cells that include floating gate transistors. The process includes: defining respective active areas for HV transistors and floating gate transistors in a semiconductor substrate, with the active areas separated from each other by insulating regions; forming insulated gate regions of the HV transistors; performing a first dopant implantation to form first portions of the HV transistor junctions; conformably depositing a dielectric layer onto the whole substrate to provide an interpoly layer of the floating gate transistor; making openings at the first portions of the HV transistor junctions; performing, through the openings, a second dopant implantation to form second portions of the high-voltage transistor junctions, with perimeter areas of the gate regions and the active area of the floating gate transistor being screened off by the dielectric layer.

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